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Frequency and Area Dependence of High-K/Ge MOS Capacitors

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Abstract – This paper investigates the capacitance-voltage (C-V) measurements of Ge/Al_2O_3/ZrO_2/TiN MOS capacitors at different frequencies for square devices with different side lengths (10 μm, 20 μm, 30 μm, 40 μm, 50 μm, 100 μm). The results show that the series resistance corrected capacitance (C_C) for accumulation region is dependent on frequency, devices substrate and area. C_C increases at a faster pace when a lower frequency (1KHz) is used than at a higher frequency (1MHz). Substantial decrease of C_C per unit area is reported in Ge/High-K in comparison to Si/High-K devices when device area is increased. This decrease is attributed to the large non-uniform interface defect density and high leakage current associated with Ge.

Introduction

Low power requirements in semiconductor devices dictate the integration of advanced high-k dielectrics with metal gates in Complementary Metal Oxide Semiconductors (CMOS) technologies (1-2). To enhance the device performance, high mobility channel materials like Ge has been extensively studied due to its bulk electron and hole mobility that are approximately two and four times higher than those of Si (3) respectively. Further enhancement of the dielectrics and interface quality can be achieved by various advanced processing and treatments during or after the deposition of high-k dielectrics (4). However, many issues of the interface between the high-k dielectrics and the high mobility substrates are yet to be resolved for the performance to exceed the silicon devices (5-7).

Making a good Ge/high-k interface is very difficult compared to Si/high-k interface. The variations in process conditions significantly impact the nature of the dielectric-semiconductor interface that controls the channel mobility. In addition, the interaction of oxygen and Ge at the interface to form GeO_x or GeO_2 further degrades the interface. Various dry and wet interface treatment and passivation techniques were used in addition to post deposition treatments to stabilize the interface. Recently, the use of slot-plane-antenna plasma oxidation (SPAO) has been studied for TiN/ZrO_2/Al_2O_3/Ge MOS capacitors, where SPAO has been introduced in different stages (before Al_2O_3 deposition, in between Al_2O_3 and ZrO_2 deposition, and after the deposition of both Al_2O_3 and ZrO_2) during the gate stack formation. It was found that, when SPAO was introduced after the deposition of both Al_2O_3 and ZrO_2, a stable GeO_2 is formed at the interface between Ge and Al_2O_3, which reduces the EOT downscaling but lowers the interface state density, D_{it}, in the devices (8). One of the biggest challenge of new process integration is the variability which can be introduced from various sources including systematic components and random components of device fabrication process in various stages (9). The systemic component

of variability is layout dependent and hence it can be predicted by analyzing the electrical characteristics (10). The active device area and perimeter of the devices have strong influence on the defect density in the dielectric and at the interface (11-12).

In this work, we are investigating the impact of active device area and perimeter on the electrical characteristics of MOS capacitors with Ge substrate where atomic layer deposited (ALD) ZrO_2/Al_2O_3 stack has been utilized as dielectric on Ge substrate. The devices studied in this work have different types of GeO_x interfacial layer formed by utilizing either SPAO oxidation in different stages of ALD deposition of ZrO_2/Al_2O_3 on chemical oxide removed (COR) processed Ge substrate or oxidation of Ge by O_3. The COR process is a non-plasma dry cleaning process. It utilizes a combination of anhydrous gaseous HF and NH_3, rather than traditional wet cleaning, to remove native oxides without damaging or roughening the sample surface (13). In addition, GeO_x formed by chemically grown oxide on Ge without any SPAO or COR process has been studied. The capacitance voltage (C-V) characteristics at different frequencies for square devices with different side lengths (10 μm, 20 μm, 30 μm, 40 μm, 50 μm, 100 μm) have been extensively studied. Furthermore, the experimental results have been compared with some theoretical models available in the literature.

Experimental Procedure

The MOS capacitors were fabricated on a 300nm Ge epitaxially grown on Si with a graded SiGe buffer layer (13). The High-K layer consists of 1nm Al_xO_y/3.5nm ZrO_q that is deposited by atomic layer deposition (ALD) while four different types of interfacial layers are used in these devices. The interfacial layers are formed by (i) simple chemical oxidation (Chemox); (ii) chemical oxide removal (COR); (iii) the native oxide on the Ge wafers was removed using TEL Certas^{TM} COR process (2) COR followed by 1 nm oxide by slot-plane-antenna (SPA) plasma (COR + $SPAO_x$); and (iv) COR followed by vapor O_3 treatment (COR+O_3). The Chemox and COR + $SPAO_x/O_3$ are wet processes. The high-k layer was deposited *in situ* in a 300nm TEL Trias^{TM} cleanroom tool. Al_2O_3 was used because it forms better interface with germanium (15) and it also has better nucleation effectively (2). ZrO_2 was used to achieve better EOT scaling and electrical performance since the dielectric constant of Al_2O_3 is not high enough (14). The ALD ZrO_2 and Al_2O_3 were grown by using tetrakis (ethymethylamido) zirconium as the Zr precursor and trimethyl aluminum as Al precursor (2) respectively. H_2O was used as oxidant at a deposition temperature of 250 ^{0}C at both cases. TiN was used as metal gate. Table-I lists all the deposition lots and Fig. 1 outlines the wafer processing for device fabrication. For comparison, silicon devices have $HfAlO_x$ as the gate dielectrics.

TABLE I. Sample Description. Cy stands for cycles. Sample 1-6 are Ge and Sample 7 is Si.

Sample Number	IL	HiK	Split
1	Chemox	1nm Al_2O_3/3.5nm ZrO_2	N/A
2	COR + $SPAO_x$ 1nm	1nm Al_2O_3/3.5nm ZrO_2	N/A
3	COR+O_3	1nm Al_2O_3/3.5nm ZrO_2	N/A
4	N/A	1nm AlO/3.5nm ZrO_2	COR+AlO(1nm)/ZrO_2(3.5nm)+$SPAO_x$
5	N/A	1nm AlO/3.5nm ZrO_2	COR+$SPAO_x$+AlO(1nm)ZrO_2(3.5nm)
6	N/A	1nm AlO/3.5nm ZrO_2	COR+AlO(1nm)+$SPAO_x$+ZrO_2(3.5nm)
7	N/A	40Cy HfAlOx	40Cy $HfAlO_x$

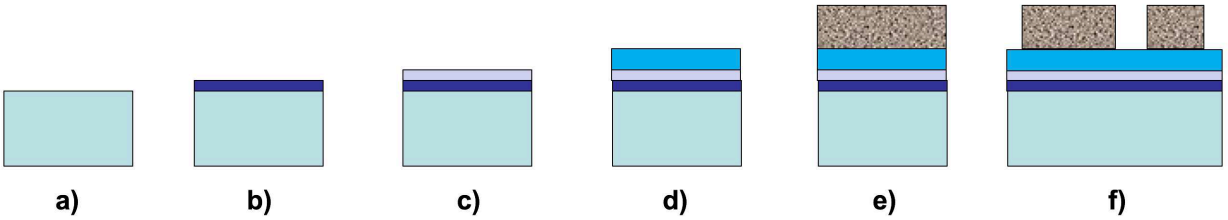

Figure 1: Device fabrication; **a)** Starting Wafer; **b)** Chemox / COR + 1nm $SPAO_x$ / COR + O_3; **c)**1nm Al_xO_y / 1nm Al_xO_y + 1nm $SPAO_x$; **d)** 3.5nm ZrO_w / 3.5nm ZrO_w + 1nm $SPAO_x$; **e,f)** TiN.

Electrical characterization of the MOS capacitors was conducted by using cascade micro-chamber with a precision probe station where HP4284 LCR meter was used for C-V measurements. MOS capacitors with six different sizes (10x10 μm, 20x20 μm, 30x30 μm, 40x40 μm, 50x50 μm, 100x100 μm) were considered where six devices were studied by capacitance voltage (C-V) characteristics at ten different frequencies (1 MHz, 500 KHz, 100 KHz, 50KHz, 25 KHz, 10 KHz, 5 KHz, 1 KHz, 500 Hz, 100 Hz). The sweep rate was very slow (approximately 5s) and it was done from inversion to accumulation region. The measurements for each device were taken as an average of 3 (three) different devices that were not leaky and located on different areas of the wafer. All measurements were taken at room temperature. Automatic Labview programs were used to enhance the efficiency in data collection and formulation. The total capacitance of each device was obtained and investigated for each device size separately.

Results and Discussion

Accumulation capacitance has a strong dependence on frequency in metal oxide semiconductor devices. Fig. 2 and Fig. 3 show the graphs of capacitance per unit area versus voltage. Measurements were performed with 1KHz (Fig. 2(a), Fig. 3(a)) and with 1MHz frequency (Fig. 2(b), Fig. 3(b)) for two different samples (sample#1 and sample#2). Higher dispersion of accumulation capacitance was observed at high frequency (1MHz) than the low frequency (1KHz) measurements. Our devices follow the same trend as previous studies have reported (14,17,18). Similar dispersion in accumulation was reported in other observations in the experimental C-V measurements at other MIS devices with substrates such as GaAs[9-10], $In_{0.53}Ga_{0.47}As$[11], InP[12], and GaSb (8). The dispersion is mainly attributed to the defects at the interface that leads to high leakage current. For the Ge/high-k devices the interface quality variation and the substrate resistance increase led to frequency dispersion as reported in previous studies (2,14,17,18).

As it can be seen from the C-V characteristics (Fig. 2 and Fig. 3), the normalized capacitance at accumulation region tends to decrease as the device area is being increased. The trend is noticeable at low frequency measurements and the dispersion is very obvious at high frequency measurements. All devices in Table I follow this trend as confirmed by their C-V characteristics graphs.

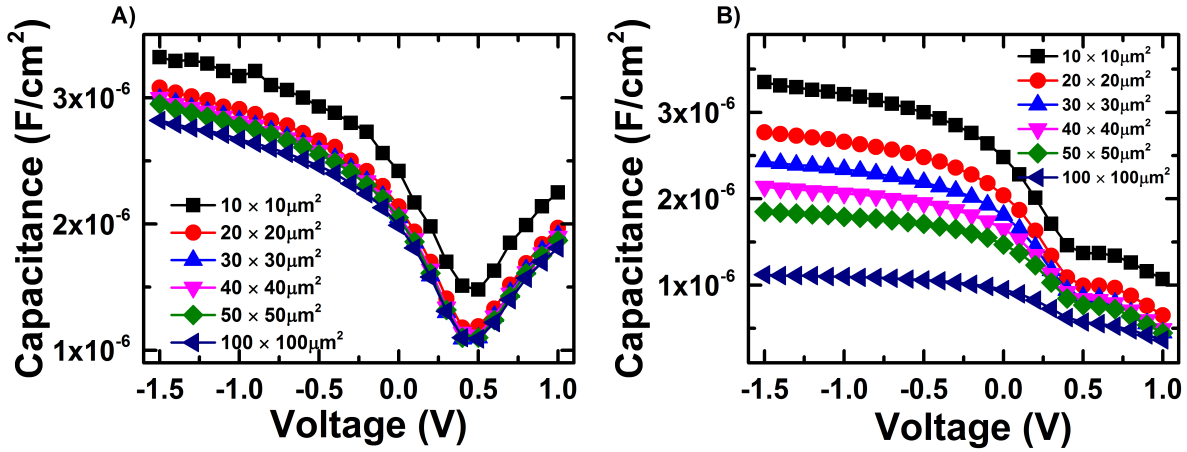

Figure 2: C-V Characteristics for Sample # 1 at **a)** 1KHz and **b)** 1MHz frequency.

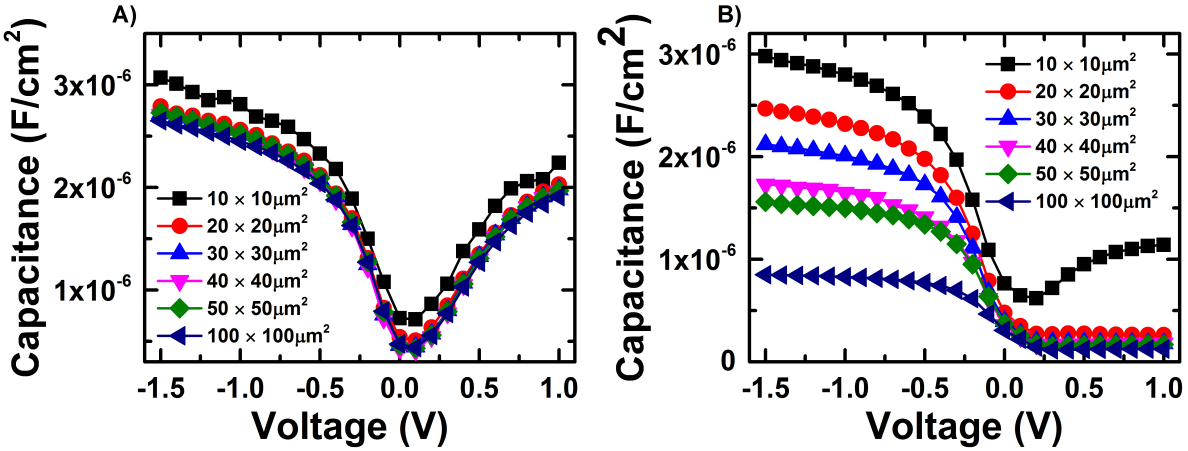

Figure 3: C-V Characteristics for Sample # 2 at **a)** 1KHz and **b)** 1MHz frequency.

The series resistance corrected capacitance (C_c) for accumulation region increases at a faster pace when a lower frequency (1KHz) is used than at a higher frequency (1MHz) (Fig. 4(a)) as a function of side length, *a*. Fig. 4(a) shows the difference in capacitance at measurements taken at 1MHz versus 1KHz frequency. It can be observed that as the device area is increased, the difference in capacitance increases as well. Let us consider samples 4, 5, and 6 and their capacitance difference. The difference in structure of these devices is where SPAO is applied. At sample 4 we have the SPAO applied after the high-k layer, sample 5 has SPAO applied before high-k layer, and sample 6 has SPAO applied between the 1nm AlO and 3.5nm ZrO_2. It appears that the greatest ΔC is observed at sample 5 and the lowest ΔC appears at sample 6 while sample 4 has ΔC in between the other two samples. According to this, we can conclude that the quality of the high-k layer is the best (lowest ΔC) when SPAO is applied between 1nm AlO and 3.5nm ZrO_2 and the worst quality is when SPAO is applied before the high-k layer. The size of the normalized capacitance is still the greatest at sample 5 for devices up to 100x100 μm (Fig.5) and the lowest can be said to be for sample 4. It can also be noted that the behavior of ΔC as a function of perimeter is almost the same for sample 1 and 4. Sample 1 has Chemox and then high-k/ALD and sample 4 has SPAO after the High-K/ALD. The identical ΔC seems to be due to

identical interfacial layer thickness (2, 8). The variations in Fig. 4(a) suggest that the frequency dispersion is highly influenced by the processing conditions. Fig. 4(b) shows corrected normalized capacitance as a function of gate voltage as measured at 1MHz at device area of 40x40 μm. As it can be seen from the graph, sample 1 (Chemox) and 3 (COR + O_3) experience the highest normalized capacitance at accumulation region because of interfacial layer thickness variation. Thinner interfacial layer thickness increases the capacitance and when the interfacial layer thickness is high, capacitance decreases as the low dielectric constant of the interfacial layer reduces the total dielectric constant. The other samples (COR + SPAO) (sample#2 and #5) have reduced interface state, D_{it}, as COR plus SPAO processed interface has relatively lower interface state than Chemox and COR + O_3 processed samples at room temperature (19). On the other hand, when SPAO was done after high-k deposition, (samples #4 and #6) the interface state density decreases with increase in thickness.

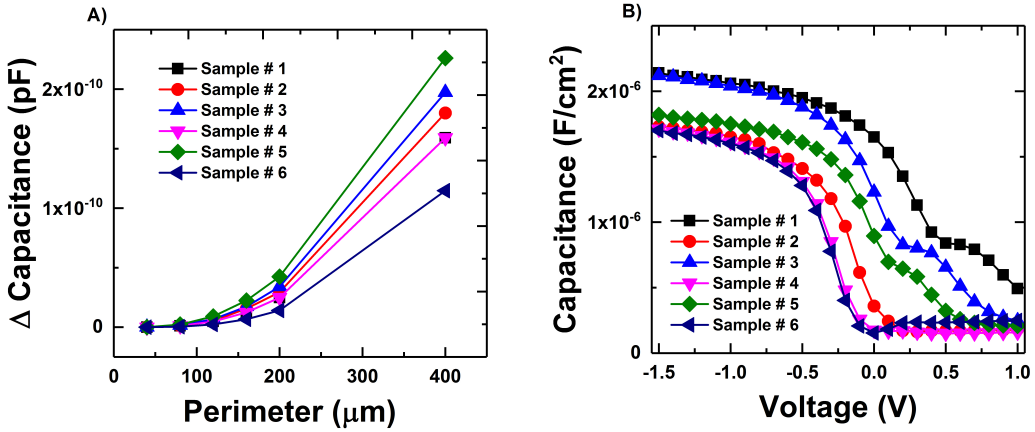

Figure 4: **a)** Capacitance Difference between measurements taken at 1 KHz and 1 MHz frequencies respectively; **b)** Corrected Normalized Capacitance versus gate voltage measured at 1MHz at device area of 40x40 μm.

Our study further shows substantial decrease of C_c per unit area in Ge/high-k in comparison to Si/high-k devices (Fig. 5) as a function of area. This decrease is mainly attributed to the large non-uniform interface defect density (19) and high leakage current associated with Ge stacks. Capacitance at accumulation condition depends on interface capacitance (C_{it}), which changes with defects density. Even if the defect density is uniform but large, it increases the leakage current proportionally with area. High-k/Ge devices with increased leakage current, therefore, experience a higher decrease of C_c per unit area compared to Si/high-k devices. This behavior is observed in Fig. 5 in the 100x100 μm devices.

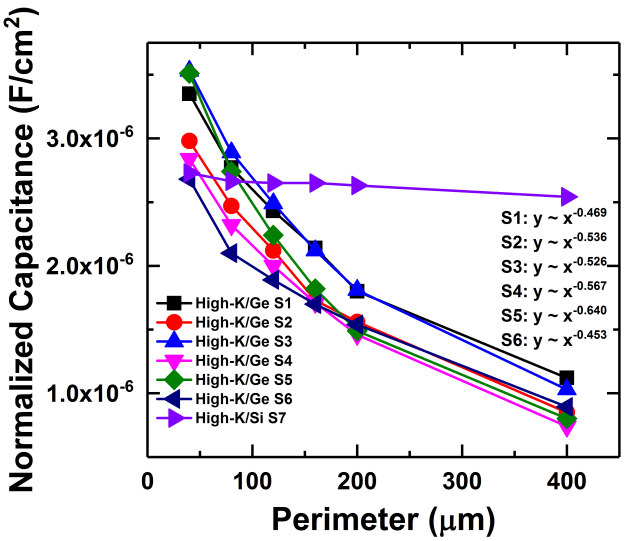

Figure 5: Capacitance per unit area is plotted as a function of perimeter for Ge substrate and Si substrate samples for measurements at frequency of 1MHz.

Inside the dielectric there are three types of charges that contribute to the capacitance: (i) fixed oxide charge due to structural defects in the dielectric; (ii) oxide trapped charge due to trapped electrons or holes in the bulk of the dielectric; and (iii) interface charge due to structural defects and by broken bonds at the interface (17). These charges are measured by taking capacitance voltage measurements with dc voltage sweep from negative to positive direction and a small ac signal with a small amplitude in the order of 10mV. The ac voltage is the one that measures the capacitance. When the amount of charges (Q_i) in the high-k/substrate interfacial layer increases, then the overall capacitance (C) will become the series connection between the oxide and interface charge capacitance. As the interface capacitance will increase with more defects, the overall capacitance will decrease. As the device area increases, the defect density increases as well since the probability of encountering defects goes up. Therefore, the normalized capacitance at Ge MOS devices as a function of device perimeter decreases at a rate ~$x^{-0.5}$ (Fig. 5).

Conclusion

This work investigated the frequency dispersion as a function of device perimeter/area in high-k/Ge devices while comparing it to Si substrate devices. The capacitance per area decrease as the device area is increased was attributed to the large non-uniform interface defect density and high leakage current in Ge devices. The accumulation capacitance has strong dependence on frequency in MOS devices and the capacitance difference (ΔC) for high (1MHz) and low (1KHz) frequency heavily depends on processing conditions, interfacial layer thickness, and quality. The interface quality has major impact on the normalized capacitance at Ge devices and the interface defect density heavily depends on the type of processing conditions.

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